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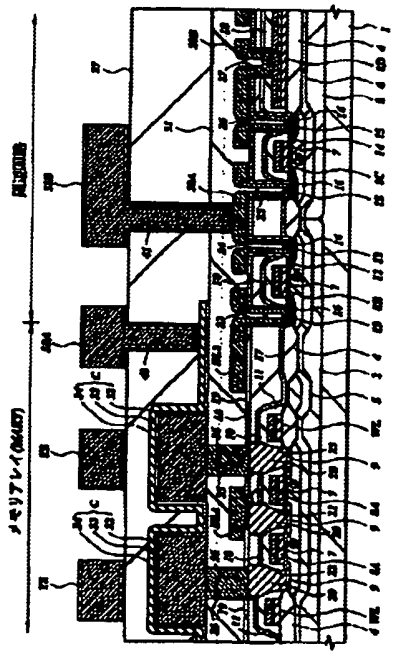
(54)【発明の名称】　半導体集積回路装置およびその製造方法

(57)【要約】

【課題】　ＣＯＢ（キャパシタ・オーバー・ビットライン）構造を有するＤＲＡＭの製造工程を簡略化し、高速化、高性能化、高集積化を推進する。

【解決手段】　メモリセル選択用ＭＩＳＦＥＴＱｔのゲート電極８Ａ（ワード線ＷＬ）、周辺回路のｎチャネル型ＭＩＳＦＥＴＱｎのゲート電極８Ｂおよびｐチャネル型ＭＩＳＦＥＴＱｐのゲート電極８Ｃを多結晶シリコンやポリサイドよりも低抵抗のＷを含む導電膜で構成し、同一工程で形成する。また、ビット線BL_1, BL_2と周辺回路の第２層目の配線３０Ａ、３０ＢとをＷを含む導電膜で構成し、同一工程で形成する。



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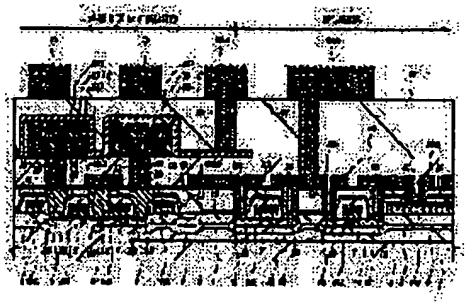
(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND MANUFACTURE THEREOF

(57)Abstract:
PROBLEM TO BE SOLVED: To advance the improvement for providing a high speed, high performance and high integration degree device by simplifying the process of manufacturing a DRAM having a capacitor over bit line structure.
SOLUTION: A W-contained conductive film having a lower resistance than that of a polysilicon or polycide is used to form gate electrodes 8A (word lines WL) of memory cell selecting MISFETs Qt, and gate electrodes 8B and 8C of n-and p-channel type MISFETs Qp for peripheral circuits in the same step. A W-contained conductive film is used to form bit lines BL1, BL2 and wirings 30A, 30B on a second layer of the peripheral circuits in the same step.



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[Claim(s)]

[Claim 1] Semiconductor integrated circuit equipment which has DRAM equipped with the memory cell of the stacked capacitor structure which arranges a bit line in the upper part of MISFET for memory cell selection, and arranges the capacitative element for information storage in the upper part of the aforementioned bit line characterized by providing the following. The word line connected to the gate electrode of the aforementioned MISFET for memory cell selection, and this. The gate electrode of MISFET of a circumference circuit. About the 1st-layer wiring of a circumference circuit, it is the metal film of at least one layer.

[Claim 2] Semiconductor integrated circuit equipment characterized by making the auxiliary wiring which is semiconductor integrated circuit equipment according to claim 1, constituted the lower electrode of the aforementioned capacitative element for information storage from the 4th conductive layer containing the metal film of at least one layer, and consisted of the lower electrodes, capacity insulator layers, and up electrodes of the aforementioned capacitative element for information storage intervene between the 2nd-layer wiring of the aforementioned circumference circuit, and the 3rd-layer wiring.

[Claim 3] It is semiconductor integrated circuit equipment characterized by the bird clapper from the metal chosen from the group which it is semiconductor integrated circuit equipment according to claim 1 or 2, and the aforementioned metal film becomes from a tungsten, aluminum, titanium, platinum, copper, and platinum.

[Claim 4] It is semiconductor integrated circuit equipment with which it is semiconductor integrated circuit equipment according to claim 1, 2, or 3, and the 1st conductive layer of the above is characterized by the bird clapper from the cascade screen of a polycrystal silicon film, a titanium night RAIDO film, and a tungsten film.

[Claim 5] The 1st-layer wiring of the aforementioned circumference circuit which is semiconductor integrated circuit equipment according to claim 4, and consisted of the 1st conductive layer of the above is semiconductor integrated circuit equipment characterized by being arranged only at the upper part f the insulator layer for

isolation.

[Claim 6] It is semiconductor integrated circuit equipment with which it is semiconductor integrated circuit equipment given in any 1 term of claims 1-5, and the 2nd conductive layer of the above is characterized by the bird clapper from the cascade screen of a titanium night RAIDO film and a tungsten film.

[Claim 7] It is semiconductor integrated circuit equipment with which it is semiconductor integrated circuit equipment given in any 1 term of claims 1-6, and the up electrode of the aforementioned capacitative element for information storage is characterized by the bird clapper from a titanium night RAIDO film.

[Claim 8] The manufacture method of semiconductor integrated circuit equipment of having DRAM equipped with the memory cell of the stacked capacitor structure which arranges a bit line in the upper part of MISFET for memory cell selection, and arranges the capacitative element for information storage in the upper part of the aforementioned bit line characterized by providing the following. (a) The word line connected to the gate electrode of MISFET for memory cell selection, and this by carrying out patterning of the 1st conductive layer of the above after forming the 1st conductive layer containing the metal film of at least one layer on a semiconductor substrate. The gate electrode of MISFET of a circumference circuit. The word line connected to the process, the gate electrode of MISFET for the (b) aforementioned memory cell selection, and this which form the 1st-layer wiring of a circumference circuit simultaneously. It is the metal film of at least one layer on the 1st insulator layer formed in the upper part of the gate electrode of MISFET of the aforementioned circumference circuit, and the 1st-layer wiring of the aforementioned circumference circuit.

[Claim 9] The manufacture method of the semiconductor integrated circuit equipment which is the manufacture method of semiconductor integrated circuit equipment according to claim 8, and is characterized by carrying out flattening of the front face of the above 1st, the 2nd, and 3rd insulator layers by the chemical mechanical-polishing method.

[Detailed Description of the Invention]

[0001]

[The technical field to which invention belongs] Especially this invention is a stacked capacitor (stacked capacitor) which arranges the capacitative element for information storage (capacitor) in the upper part of MISFET for memory cell selection about semiconductor integrated circuit equipment and its manufacturing technology. It applies to the semiconductor integrated circuit equipment which has DRAM (Dynamic

Random Access Memory) equipped with the memory cell of structure, and is related with effective technology.

[0002]

[Description of the Prior Art] The large capacity DRAM in recent years has adopted the stacked capacitor structure which arranges the capacitative element for information storage in the upper part of MISFET for memory cell selection, in order to compensate reduction of the amount of stored charges of the capacitative element for information storage accompanying detailed-izing of a memory cell (Cs).

[0003] The capacitative element for information storage of stacked capacitor structure carries out the laminating of an accumulation electrode (lower electrode), a capacity insulator layer, and the plate electrode (up electrode) one by one, and is formed. The accumulation electrode of the capacitative element for information storage is connected to one side of the semiconductor region (a source field, drain field) of MISFET for memory cell selection which consisted of n channel types. A plate electrode is constituted as an electrode common to two or more memory cells, and predetermined fixed potential (plate potential) is supplied.

[0004] The bit line for performing writing of data and read-out is connected to another side of the semiconductor region (a source field, drain field) of MISFET for memory cell selection. A bit line is arranged between MISFET for memory cell selection, and the capacitative element for information storage, or at the upper part of the capacitative element for information storage. The structure which arranges the capacitative element for information storage in the upper part of a bit line is called capacitor over bit-line (Capacitor Over Bitlinne; COB) structure.

[0005] About DRAM which has the above-mentioned COB structure, JP,7-122654,A and JP,7-106437,A have a publication.

[0006] DRAM indicated by JP,7-122654,A The bit line formed in the upper part of MISFET for memory cell selection which formed the gate electrode (word line) by the cascade screen (polycide film) of a polycrystal silicon film or a polycrystal silicon film, and a tungsten silicide (WSix) film by the polycrystal silicon film (or polycide film) is arranged. The capacitative element for information storage which consists of the accumulation electrode formed in the upper part of this bit line by the polycrystal silicon film, a capacity insulator layer formed by the cascade screen of a silicon-oxide film and a silicon nitride film, and a plate electrode formed by the polycrystal silicon film is arranged. And the common-source line formed in the upper part of this capacitative element for information storage by aluminum (aluminum) film of the 1st layer and the word line for shunts formed by aluminum film of the 2nd layer are arranged.

[0007] DRAM indicated by JP,7-106437,A arranges the bit line formed in the upper part of MISFET for memory cell selection which formed the gate electrode (word line) by the polycrystal silicon film by the polycide film. And by forming simultaneously the accumulation electrode of the capacitative element for information storage or plate electrode arranged in the upper part of this bit line, and the 1st-layer wiring of a circumference circuit with metal material (for example, Pt (platinum)), the electrode formation process of the capacitative element for information storage and the metal wiring formation process of a circumference circuit are communalized, and simplification of a manufacturing process is attained.

[0008]

[Problem(s) to be Solved by the Invention] Since resistance forms the gate electrode (word line) by high polycrystal silicon and a high polycide compared with metal material, such as aluminum and W, DRAM of the COB structure mentioned above is reducing the gate delay by forming the metal wiring for gate electrode backing (word line for shunts) in the upper part of the capacitative element for information storage. Moreover, resistance is high, and since the bit line is formed by polycrystal silicon and the polycide which moreover are not simultaneously connectable with n type substrate and p type substrate, a bit line and wiring of a circumference circuit cannot be communalized. Therefore, the number of each wiring layers of a memory array and a circumference circuit increases, and the problem that a manufacturing process increases arises.

[0009] Moreover, if the number of wiring layers increases, the number of layers of the layer insulation film formed between up-and-down wiring will also increase, and the number of times of the flattening processing which carries out a reflow of the layer insulation film, or anneals it at the elevated temperature of 850-900 degrees C increases. Therefore, as a result of it becoming difficult to become easy to diffuse in a substrate the impurity's in the semiconductor region (diffusion layer's) which constitutes the source field's of MISFET and a drain field's, and it to form shallow pn junction's, the problem that the performance of MISFET falls arises.

[0010] Moreover, since a bit line and wiring of a circumference circuit cannot be communalized, you have to form the 1st-layer wiring of a circumference circuit in the upper layer rather than a bit line. therefore, the connection which connects the 1st-layer wiring and MISFET of a circumference circuit -- the result to which the aspect ratio (a path/depth) of a hole becomes large -- connection -- that formation of a hole becomes difficult **** -- connection -- the problem that it becomes difficult to embed a wiring material to the interior of a hole arises

[0011] Moreover, when resistance forms a gate electrode (w rd line) by high polycrystal

silicon and a high polycide, the number of memory cells which can connect with one WORD driver cannot be made [many]. That is, since the number of the WORD drivers connected to a predetermined number of memory cells must be made [many] in order to reduce a gate delay, the problem that a chip size becomes large and a degree of integration falls arises.

[0012] One purpose of this invention is to offer the technology which can simplify the manufacturing process of DRAM which has COB structure.

[0013] Other purposes of this invention are to offer the technology in which the improvement in the speed of DRAM which has COB structure can be promoted.

[0014] Other purposes of this invention are to offer the technology in which highly efficient-ization of DRAM which has COB structure can be promoted.

[0015] Other purposes of this invention are to offer the technology in which the high integration of DRAM which has COB structure can be promoted.

[0016] The other purposes and the new feature will become clear from description and the accompanying drawing of this specification at the aforementioned row of this invention.

[0017]

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.

[0018] (1) The semiconductor integrated circuit equipment of this invention arranges a bit line in the upper part of MISFET for memory cell selection. The word line which has DRAM which equipped the upper part of the aforementioned bit line with the memory cell of the stacked capacitor structure which arranges the capacitative element for information storage, and is connected to the gate electrode of the aforementioned MISFET for memory cell selection, and this, The gate electrode of MISFET of a circumference circuit, and the 1st-layer wiring of a circumference circuit It constitutes from the 1st conductive layer containing the metal film of at least one layer. the aforementioned bit line and the 2nd-layer wiring of a circumference circuit It constitutes from the 2nd conductive layer containing the metal film of at least one layer, and wiring of the upper part of the aforementioned capacitative element for information storage and the 3rd-layer wiring of a circumference circuit consist of the 3rd conductive layer containing the metal film of at least one layer.

[0019] (2) The manufacture method of the semiconductor integrated circuit equipment of this invention (a) after forming the 1st conductive layer containing the metal film of at least one layer on a semiconductor substrate, by carrying out patterning of the 1st conductive layer of the above The word line connected to the gate electrode of MISFET

for memory cell selection, and this, The word line connected to the process, the gate electrode of MISFET for the (b) aforementioned memory cell selection, and this which form simultaneously the gate electrode of MISFET of a circumference circuit, and the 1st-layer wiring of a circumference circuit, After forming the 2nd conductive layer containing the metal film of at least one layer on the 1st insulator layer formed in the upper part of the gate electrode of MISFET of the aforementioned circumference circuit, and the 1st-layer wiring of the aforementioned circumference circuit, The process which forms simultaneously a bit line and the 2nd-layer wiring of a circumference circuit by carrying out patterning of the 2nd conductive layer of the above, (c) on the 2nd insulator layer formed in the upper part of the aforementioned bit line and the 2nd-layer wiring of the aforementioned circumference circuit The process which forms the capacitative element for information storage which consists of a lower electrode, a capacity insulator layer, and an up electrode, (d) after forming the 3rd conductive layer containing the metal film of at least one layer on the 3rd insulator layer formed in the upper part of the aforementioned capacitative element for information storage, by carrying out patterning of the 3rd conductive layer of the above The process which forms simultaneously wiring of the upper part of the aforementioned capacitative element for information storage and the 3rd-layer wiring of a circumference circuit is included.

[0020]

[Embodiments of the Invention] Hereafter, the gestalt of operation of this invention is explained in detail based on a drawing. In addition, what has the same function in the complete diagram for explaining the gestalt of operation attaches the same sign, and explanation of the repeat is omitted.

[0021] (Gestalt 1 of operation) The whole semiconductor chip plan with which drawing 1 formed DRAM of the gestalt of this operation, and drawing 2 are the expansion plans showing the part.

[0022] DRAM which has the capacity of for example, 64Mbit(s) (megabit) is formed in the principal plane of semiconductor chip 1A which consists of single crystal silicon. As shown in drawing 1, this DRAM consists of a memory mat MM divided into eight pieces, and a circumference circuit arranged at those circumferences. 8Mbit(s) Each of the memory mat MM which has capacity is divided into 16 memory arrays MARY as shown in drawing 2 . Each of the memory array MARY is 2Kbit x(kilobit)256bit =512Kbit arranged in the shape of a matrix. It consists of memory cells and the sense amplifier SA and the WORD driver WD of a circumference circuit are arranged at those circumferences.

[0023] Drawing 3 is the cross section f a semiconductor substrate showing the

important section (one section each of the circumference circuit which adjoins the memory array shown in drawing 2 , and it) of DRAM of the gestalt of this operation.

[0024] p- p type common to the memory array MARY and a circumference circuit to the semiconductor substrate 1 which consists of single crystal silicon of a mold -- n type of a well 2 and a circumference circuit -- the well 3 is formed p type -- a well 2 and n type -- p type which the field oxide film 4 for isolation is formed in each front face of a well 3, and contains the lower part of this field oxide film 4 -- the inside of a well 2 -- p type channel-stopper layer 5 -- moreover, n type -- in the well 3, n type channel-stopper layer 6 is formed, respectively

[0025] p type of the memory array MARY -- the memory cell (plurality) is formed in the active field of a well 2 Each of a memory cell consists of capacitative element C for information storage of the piece formed in MISFETQt for memory cell selection and the upper part of the piece which consisted of n channel types. That is, this memory cell consists of stacked capacitor structures which arrange the capacitative element C for information storage in the upper part of MISFETQt for memory cell selection.

[0026] MISFETQt for memory cell selection consists of gate electrode 8A formed in the gate oxide film 7, a word line WL, and one, and n-type-semiconductor fields 9 and 9 (a source field, drain field) of a couple. Gate electrode 8A (word line WL) consists of electric conduction films (the 1st conductive layer) of three layers which carried out the laminating of a polycrystal silicon film, a TiN (titanium night RAIDO) film, and the W (tungsten) film, and in order to reduce the resistance, the n type impurity (P (Lynn)) is doped by the polycrystal silicon film. The silicon nitride film 10 is formed in the upper part of gate electrode 8A (word line WL), and the sidewall spacer 11 of a silicon nitride is formed in the side attachment wall.

[0027] p type of a circumference circuit -- n channel type MISFETQn forms in the active field of a well 2 -- having -- **** -- n type -- p-channel type MISFETQp is formed in the active field of a well 3 That is, this circumference circuit is CMOS (Complementary Metal Oxide Semiconductor) which combined n channel type MISFETQn and p-channel type MISFETQp. It consists of circuits.

[0028] N channel type MISFETQn consists of the gate oxide film 7, gate electrode 8B, a source field, and a drain field. Gate electrode 8B consists of electric conduction films of three layers which carried out the laminating of a polycrystal silicon film, a TiN film, and the W film as well as gate electrode 8A (word line WL) of the aforementioned MISFETQt for memory cell selecti n. Moreover, the silicon nitride film 10 is formed in the upper part of gate electrode 8B, and the sidewall spacer 11 of a silicon nitride is formed in the side attachment wall. A source field and a drain field are n of low high

impurity concentration. · The type semiconductor region 12 and n+ of high high impurity concentration LDD which consists of a type semiconductor region 13 (Lightly Doped Drain) It consists of structures and is n+. Ti silicide (TiSix) layer 16 is formed in the front face of the type semiconductor region 13.

[0029] P-channel type MISFETQp consists of the gate oxide film 7, gate electrode 8C, a source field, and a drain field. Gate electrode 8C consists of electric conduction films of three layers which carried out the laminating of a polycrystal silicon film, a TiN film, and the W film as well as gate electrode 8A (word line WL) of the aforementioned MISFETQt for memory cell selection. Moreover, the silicon nitride film 10 is formed in the upper part of gate electrode 8C, and the sidewall spacer 11 of a silicon nitride is formed in the side attachment wall. A source field and a drain field are p of low high impurity concentration. · The type semiconductor region 14 and p+ of high high impurity concentration It consists of LDD structures which consist of a type semiconductor region 15, and is p+. Ti silicide layer 16 is formed in the front face of the type semiconductor region 15.

[0030] Wiring 8D of the 1st layer is formed in the upper part of the field insulator layer 4 of a circumference circuit. Wiring 8D consists of electric conduction films of three layers which carried out the laminating of a polycrystal silicon film, a TiN film, and the W film as well as gate electrode 8A (word line WL) of the aforementioned MISFETQt for memory cell selection. Moreover, the silicon nitride film 10 is formed in the upper part of wiring 8D, and the sidewall spacer 11 of a silicon nitride is formed in the side attachment wall.

[0031] The silicon-oxide film 17 is formed in the upper part of MISFETQt for memory cell selection, n channel type MISFETQn, p-channel type MISFETQp, and wiring 8D. The BPSG (Boron-doped Phospho Silicate Glass) film 18 is formed in the upper part of the silicon-oxide film 17, and the silicon-oxide film 19 is formed in the upper part of the BPSG film 18.

[0032] Bit lines BL1 and BL2 are formed in the upper part of the silicon-oxide film 19 of the memory array MARY. Bit lines BL1 and BL2 It consists of two-layer electric conduction films (the 2nd conductive layer) which carried out the laminating of a TiN film and the W film. bit line BL1 the connection which embedded the plug 20 of polycrystal silicon -- the source field of MISFETQt for memory cell selection and the drain field are electrically connected with on the other hand (n-type-semiconductor field 9) through the hole 21 moreover, bit line BL2 connection -- the source field of n channel type MISFETQn of a circumf rence circuit and the drain field are electrically connected with on the other hand (n+ type semiconductor region 13) through the hole 23

[0033] The 2nd-layer wiring 30A and 30B is formed in the upper part of the silicon-oxide film 19 of a circumference circuit. Wiring 30A and 30B is the aforementioned bit lines BL1 and BL2. Similarly it consists of two-layer electric conduction films which carried out the laminating of a TiN film and the W film. the end of wiring 30A -- connection -- it connects with another side (n+ type semiconductor region 13) of the source field of n channel type MISFETQn, and a drain field electrically through a hole 24 -- having -- **** -- the other end -- connection -- the source field of p-channel type MISFETQp and the drain field are electrically connected with on the other hand (p+ type semiconductor region 15) through the hole 25 moreover, the end of wiring 30B -- connection -- it connects with another side (p+ type semiconductor region 15) of the source field of p-channel type MISFETQp, and a drain field electrically through a hole 26 -- having -- **** -- the other end -- connection -- it connects with wiring 8D of the 1st aforementioned layer electrically through the hole 27

[0034] As shown in drawing 4 (plan showing a part of other circumference circuits), the circumference circuit of DRAM of the gestalt of this operation is connecting n channel type MISFETQn and p-channel type MISFETQp using wiring 8D of the 1st layer, and the 2nd-layer wiring 30C-30G. wiring 8D of the 1st layer which consisted of cascade screens of the polycrystal silicon film and TiN film which doped the n type impurity (P), and W film -- p type -- a well 2 and n type -- since it is not simultaneously connectable with a well 3, it is arranged at the upper part of the field oxide film 4 Supply of the supply voltage (Vcc or GND) to n channel type MISFETQn and p-channel type MISFETQp is performed using the 3rd-layer wiring (38C, 38D) mentioned later.

[0035] Bit lines BL1 and BL2 And the silicon-oxide film 31 is formed in the upper part of Wiring 30A and 30B. The capacitative element C for information storage is formed in the upper part of the silicon-oxide film 31 of the memory array MARY. The capacitative element C for information storage consists of an accumulation electrode (lower electrode) 32, a capacity insulator layer 33, and a plate electrode (up electrode) 34.

[0036] the connection which the accumulation electrode 32 of the capacitative element C for information storage consists of W films, and embedded the plug 35 of W -- the connection which embedded the plug 20 of a hole 36 and polycrystal silicon -- it connects with another side (n-type-semiconductor field 9) of the source field of MISFETQt for memory cell selection, and a drain field electrically through the hole 22 The capacity insulator layer 33 consists of Ta2 O5 films (tantalum oxide), and the plate electrode 34 consists of TiN films.

[0037] The silicon-oxide film 37 is formed in the upper part of the capacitativ element C for information storage. Y selection line YS and wiring 38A are formed in the upper

part of the silicon oxide film 37 of the memory array MARY, and wiring 38B of the 3rd layer is formed in the upper part of the silicon oxide film 37 of a circumference circuit. wiring 38A -- connection -- it connects with the plate electrode 34 of the capacitative element C for information storage electrically through the hole 40, and plate voltage (pinch off voltage) is supplied to the plate electrode 34 wiring 38B -- connection -- it connects with wiring 30A of the 2nd layer of a circumference circuit electrically through the hole 41, and supply voltage (Vcc or GND) is supplied to MISFET of a circumference circuit Y selection line YS and Wiring 38A and 38B consist of electric conduction films (the 3rd conductive layer) of four layers which carried out the laminating of Ti film, a TiN film, aluminum (aluminum) alloy film that added Si (silicon) and Cu (copper), and the TiN film.

[0038] Those illustration is omitted, although the passivation film which consisted of cascade screens of a silicon oxide film and a silicon nitride film etc. is formed in the upper part of Y selection line YS and Wiring 38A and 38B and protective coats, such as polyimide resin, are formed in the upper part of a passivation film if needed.

[0039] Next, the manufacture method of DRAM of the gestalt this operation is explained in detail using drawing 5 - drawing 18 .

[0040] First, as shown in drawing 5 , after forming the field oxide film 4 in the front face of the semiconductor substrate 1 by the selective oxidation (LOCOS) method, Carry out the ion implantation of the p type impurity (boron (B)) to the semiconductor substrate 1 of the field which forms the memory array MARY, and the field which forms n channel type MISFET of a circumference circuit, and a well 2 is formed p mold. The ion implantation of the n type impurity (Lynn (P)) is carried out to the semiconductor substrate 1 of the field which forms p channel type MISFET of a circumference circuit, and a well 3 is formed n mold. then, p type -- a well 2 -- p type impurity (B) -- an ion implantation -- carrying out -- p type channel-stopper layer 5 -- forming -- n type -- the ion implantation of the n type impurity (P) is carried out to a well 3, and n type channel-stopper layer 6 is formed then, p type surrounded by the field oxide film 4 -- a well 2 and n type -- the gate oxide film 7 is formed in the front face of each active region of a well 3 by the oxidizing [thermally] method

[0041] Next, as shown in drawing 6 , gate electrode 8A (word line WL) of MISFETQt for memory cell selection, gate electrode 8B of n channel type MISFETQn, gate electrode 8C of p channel type MISFETQp, and wiring 8D of the 1st layer are formed. After the gate electrodes 8A (word line WL), 8B, and 8C and wiring 8D deposit a polycrystal silicon film in CVD first, subsequently deposit a TiN film and W film by the sputtering method and deposit a silicon nitride film 10 in CVD further, by etching which used the

photoresist as the mask, they carry out patterning of these films, and form them simultaneously.

[0042] next, it is shown in drawing 7 -- as -- p type -- a well 2 -- n type impurity (P) -- an ion implantation -- carrying out -- n- of the n-type-semiconductor fields 9 and 9 of MISFETQt for memory cell selection, and n channel type MISFETQn the type semiconductor region 12 -- forming -- n type -- a well 3 -- p type impurity (B) -- an ion implantation -- carrying out -- p- of p-channel type MISFETQp A type semiconductor region is formed.

[0043] Next, as shown in drawing 8 , the sidewall spacer 11 is formed in each side attachment wall of gate electrode 8A (word line WL) of MISFETQt for memory cell selection, gate electrode 8B of n channel type MISFETQn, gate electrode 8C of p-channel type MISFETQp, and wiring 8D of the 1st layer. The sidewall spacer 11 carries out anisotropic etching of the silicon nitride film deposited in CVD, and forms it. subsequently, p type of a circumference circuit -- a well 2 -- n type impurity (P) -- an ion implantation -- carrying out -- n+ of n channel type MISFETQn the type semiconductor region 13 -- forming -- n type -- a well 3 -- p type impurity (B) -- an ion implantation -- carrying out -- p+ of p-channel type MISFETQp The type semiconductor region 15 is formed.

[0044] Next, as shown in drawing 9 , after depositing the silicon-oxide film 17 and the BPSG film 18 on each upper part of gate electrode 8A (word line WL) of MISFETQt for memory cell selection, gate electrode 8B of n channel type MISFETQn, gate electrode 8C of p-channel type MISFETQp, and wiring 8D of the 1st layer in CVD, the BPSG film 18 is ground by the chemical mechanical-polishing method (Chemical Mechanical Polishing; CMP) method, and flattening of the front face is carried out.

[0045] Next, as shown in drawing 10 , after depositing the polycrystal silicon film 28 in CVD on the BPSG film 18, By using a photoresist as a mask and **********ing the polycrystal silicon film 28, the BPSG film 18, the silicon-oxide film 17, and the gate oxide film 7 the upper part [on the other hand / (n-type-semiconductor field 9)] of the source field of MISFETQt for memory cell selection, and a drain field -- connection -- a hole 21 -- forming -- the upper part of another side (n-type-semiconductor field 9) -- connection -- a hole 22 is formed connection of a path smaller than the resolution of the exposure light used for forming the mask of the above-mentioned photoresist since the sidewall spacer 11 of the silicon nitride film 10 formed in the upper part of gate electrode 8A (word line WL) of MISFETQt for memory cell selection and the silicon nitride formed in the side attachment wall remains at this time, without hardly **********ing -- holes 21 and 22 can be formed by self-adjustment (self aryne)

[0046] next, it is shown in drawing 11 -- as -- connection -- the plug 20 of polycrystal silicon is formed in the interior of holes 21 and 22 This plug 20 removes and forms the upside polycrystal silicon film and the upside polycrystal silicon film 28 of the BPSG film 18 by etchback, after depositing a polycrystal silicon film on the upper part of the polycrystal silicon film 28 in CVD. An n type impurity (P) is doped on the polycrystal silicon film which constitutes a plug 20. this impurity -- connection -- it is spread through holes 21 and 22 to the n-type-semiconductor fields 9 and 9 (a source field, drain field) of MISFETQt for memory cell selection, and the n-type-semiconductor fields 9 and 9 are formed into low resistance

[0047] next, etching which deposited the silicon-oxide film 19 on the upper part of the BPSG film 18 in CVD, and carried out the photoresist subsequently to a mask as shown in drawing 12 -- connection, as shown in drawing 13 , after removing the silicon-oxide film 19 of the upper part of a hole 21 By using a photoresist as a mask and **********ing the silicon-oxide film 19, the BPSG film 18, the silicon-oxide film 17, and the gate oxide film 7 of a circumference circuit one upper part of the source field of n channel type MISFETQn, and a drain field -- connection -- a hole 23 -- forming -- the upper part of another side -- connection -- a hole 24 is formed moreover, one upper part of the source field of p-channel type MISFETQp, and a drain field -- connection -- a hole 25 -- forming -- the upper part of another side -- connection -- a hole 26 -- forming -- the upper part of wiring 8D -- connection -- a hole 27 is formed

[0048] next, it is shown in drawing 14 -- as -- connection -- n+ of n channel type MISFETQn exposed to the pars basilaris ossis occipitalis of holes 23 and 24 With the front face of the type semiconductor region 13 connection -- p+ of p-channel type MISFETQp exposed to the pars basilaris ossis occipitalis of holes 25 and 26 After forming Ti silicide layer 16 in the front face of the type semiconductor region 15 They are bit lines BL1 and BL2 to the upper part of the silicon-oxide film 19 of the memory array MARY. It forms and the 2nd-layer wiring 30A and 30B is formed in the upper part of the silicon-oxide film 19 of a circumference circuit. After Ti silicide layer's 16 annealing Ti film deposited by the sputtering method and making it react with Si substrate (n+ type semiconductor region 13, p+ type semiconductor region 15), it removes and forms unreacted Ti film by etching. Bit lines BL1 and BL2 And by etching which used the photoresist as the mask, patterning of these films is carried out and Wiring 30A and 30B forms them simultaneously, after depositing a TiN film and W film by the sputtering method.

[0049] Next, as shown in drawing 15 , they are bit lines BL1 and BL2. And wiring 30A, By using a photoresist as a mask and **********ing the silicon-oxide film 31 and the

silicon-oxide film 19, after grinding the silicon-oxide film 31 deposited on the upper part of 30B in CVD by the chemical mechanical-polishing method and carrying out flattening of the front face the aforementioned connection formed in the upper part of another side (n-type-semiconductor field 9) of the source field of MISFETQt for memory cell selection, and a drain field -- the upper part of a hole 22 -- connection -- a hole 36 is formed

[0050] next, it is shown in drawing 16 -- as -- connection -- the connection after forming the plug 35 of W in the interior of a hole 36 -- the accumulation electrode 32 of the capacitative element C for information storage is formed in the upper part of a hole 36 The plug 35 of W carries out etchback of the W film deposited in the sputtering method and CVD to the upper part of the silicon-oxide film 31, and forms it in it. By etching which used the photoresist as the mask, patterning of the W film deposited on the upper part of the silicon-oxide film 31 by the sputtering method is carried out, and the accumulation electrode 32 forms it.

[0051] Next, as shown in drawing 17 , it is Ta 2O5 at CVD to the upper part of the accumulation electrode 32. A film is deposited. Subsequently, Ta 2O5 By carrying out patterning of these films by etching which used the photoresist as the mask, after depositing a TiN film on the membranous upper part in CVD The accumulation electrode 32 and Ta 2O5 which consisted of W films The capacitative element C for information storage which consists of a plate electrode 34 which consisted of a capacity insulator layer 33 which consisted of films, and a TiN film is formed.

[0052] Next, as shown in drawing 18 , after grinding the silicon-oxide film 37 deposited on the upper part of the capacitative element C for information storage in CVD by the chemical mechanical-polishing method and carrying out flattening of the front face, By using a photoresist as a mask and **********ing the silicon-oxide film 37 the upper part of the plate electrode 34 of the capacitative element C for information storage -- connection -- forming a hole 40 and **********ing the silicon-oxide film 37 and the silicon-oxide film 31 simultaneously -- the upper part of wiring 30A of the 2nd layer of a circumference circuit -- connection -- a hole 41 is formed

[0053] Then, DRAM shown in aforementioned drawing 3 is completed by forming Y selection line YS and the wiring 38A and 38B of the 3rd layer of a circumference circuit in the upper part of the silicon-oxide film 37. By etching which used the photoresist as the mask, patterning of these films is carried out and Y selection line YS and Wiring 38A and 38B form them simultaneously, after depositing Ti film, a TiN film, aluminum alloy film, and a TiN film on the upper part of the silicon-oxide film 37 by the sputtering method.

[0054] According to the DRAM f the form of this operation constituted as mentioned

above, the following effects can be acquired.

[0055] (1) Since a gate delay can be reduced by having constituted gate electrode 8A (word line WL) of MISFETQt for memory cell selection, gate electrode 8B of n channel type MISFETQn of a circumference circuit, and gate electrode 8C of p-channel type MISFETQp from polycrystal silicon or a polycide by the electric conduction film containing W of low resistance, the working speed of DRAM can be raised. Moreover, since the low resistance metal wiring for gate electrode backing (word line for shunts) currently formed in the upper part of the capacitative element for information storage becomes unnecessary conventionally, the wiring layer of the memory array MARY can be reduced by one layer.

[0056] (2) By the above (1), the gate electrodes 8B and 8C of gate electrode 8A (word line WL) of the memory array MARY and a circumference circuit and wiring 8D of the 1st layer can be formed at the same process. Thereby, conventionally, since the 1st-layer wiring of the circumference circuit currently formed in the wiring layer other than the wiring layer of the memory array MARY becomes unnecessary, the wiring layer of a circumference circuit can be reduced by one layer.

[0057] (3) By the above (1), the number of memory cells linked to one WORD driver WD can be made [many]. that is, since the number of the WORD drivers WD connected to a predetermined number of memory cells can be reduced, the part and a chip size can be reduced and the degree of integration of DRAM (or the occupancy area of the memory array MARY ·· expanding) can be raised

[0058] (4) Bit lines BL1 and BL2 Since bit line delay can be reduced by having constituted from an electric conduction film containing W of low resistance, the working speed of DRAM can be raised.

[0059] (5) By the above (4), they are the bit lines BL1 and BL2 of the memory array MARY. The wiring 30A and 30B of the 2nd layer of a circumference circuit can be formed at the same process. Since the 2nd-layer wiring of the circumference circuit which this formed at the process after forming the capacitative element C for information storage of a memory cell conventionally becomes unnecessary, the wiring layer of a circumference circuit can be reduced by one layer.

[0060] (6) Wiring 8D of the 1st layer and wiring 30A of the 2nd layer which connect n channel type MISFETQn and p-channel type MISFETQp of a circumference circuit, By having arranged 30B in the lower layer from the capacitative element C for information storage of a memory cell the connection formed in the upper part of the source field of n channel type MISFETQn, and a drain field ·· holes 23 and 24 and the source field of p-channel type MISFETQp ·· the connection formed in the upper part of a drain field ··

since the aspect ratio of holes 25 and 26 can be made small -- these c nnection -- the connection reliability of the wiring in the interior of a hole (23-26) can be raised

[0061] (7) Since the wiring layer of the memory array MARY can be reduced by one layer and the wiring layer of a circumference circuit can be reduced by two layers by the above (1), (2), and (5), the number of manufacturing processes of DRAM can be reduced and improvement in the yield and reduction of a manufacturing cost can be aimed at.

[0062] (8) Gate electrode 8A of MISFETQt for memory cell selection (word line WL), The BPSG film 18 deposited on the upper part of gate electrode 8B of n channel type MISFETQn, gate electrode 8C of p-channel type MISFETQp, and wiring 8D of the 1st layer, Bit lines BL1 and BL2 And the silicon-oxide film 31 deposited on the upper part of Wiring 30A and 30B, The number of the heat treatment processes of the whole process can be reduced by having ground the silicon-oxide film 37 deposited on the upper part of the capacitative element C for information storage by the chemical mechanical-polishing method, and having carried out flattening of those front faces, and the above (7). Since diffusion of the impurity in each source field of MISFETQt for memory cell selection, n channel type MISFETQn, and p-channel type MISFETQp and a drain field can be suppressed and shallow pn junction can be formed by this, detailed-izing of these MISFET(s) and highly efficient-ization can be promoted.

[0063] (Form 2 of operation) Drawing 19 is the cross section of a semiconductor substrate showing the important section of DRAM of the form of this operation.

[0064] DRAM of the form of this operation The source field of MISFETQt for memory cell selection, a drain field -- on the other hand (n-type-semiconductor field 9) -- bit line BL1 the connection connected electrically -- the interior of a hole 21, and a source field -- the connection which connects electrically another side (n-type-semiconductor field 9) of a drain field, and the accumulation electrode (lower electrode) 32 of the capacitative element C for information storage -- the plug 29 which consisted of two-layer electric conduction films which carried out the laminating of a TiN film and the W film to the interior of a hole 22 is embedded After this plug 29 deposits a TiN film and W film by the sputtering method on the silicon-oxide film 19, it carries out etchback of these films, and forms them.

[0065] According to the above-mentioned composition, the wiring layer (word line WL) of the memory array MARY, i.e., gate electrode 8of MISFETQt for memory cell selection A, Bit lines BL1 and BL2 and Y selection line YS, and plugs 29 and 35 are constituted from a conductive layer containing a low resistanc metal film (W film or aluminum film). The wiring layer of a circumference circuit, i.e., gate electrode 8of n channel type MISFETQn B, By having constituted gate electrode 8C of p-channel type MISFETQp,

wiring 8D of the 1st layer, the 2nd-layer wiring 30A and 30B, and the 3rd-layer wiring 30A and 30B from a conductive layer containing a low resistance metal film (W film or aluminum film). The working speed of DRAM can be raised.

[0066] Moreover, DRAM of the gestalt of this operation forms the auxiliary wiring 39A, 39B, and 39C between the wiring 30A and 30B of the 2nd layer of a circumference circuit, and the 3rd-layer wiring 38A and 38B. The auxiliary wiring 39A, 39B, and 39C is W film and Ta 2O5 as well as the capacitative element C for information storage. It constitutes from three layer membranes which carried out the laminating of a film and the TiN film, and forms simultaneously at the process which forms the capacitative element C for information storage.

[0067] The auxiliary wiring 39A and 39B is used as a pad layer which connects the 3rd-layer wiring 38A and 38B and the 2nd-layer wiring 30A and 30B. the connection which connects the 3rd-layer wiring 38A and 38B and the 2nd-layer wiring 30A and 30B by this -- since the aspect ratio of a hole can be made small, the connection reliability of wiring of a circumference circuit can be raised Auxiliary wiring 39C is used as dummy wiring for easing the difference in elevation of for example, the memory array MARY and a circumference circuit, and is suitably arranged to the field in which the above-mentioned pad layer is not formed.

[0068] As mentioned above, although invention made by this invention person was concretely explained based on the form of operation, it cannot be overemphasized by this invention that it can change variously in the range which is not limited to the form of the aforementioned implementation and does not deviate from the summary.

[0069] For example, the gate electrode (word line) of MISFET, and the 1st-layer wiring of a circumference circuit or the accumulation electrode of the capacitative element for information storage may consist of conductive layers containing WN (nitriding tungsten) film. Moreover, the plate electrode of the capacitative element for information storage may be constituted from a conductive layer containing Pt (platinum) or Au(gold), or a capacity insulator layer may consist of ferroelectric films, such as PZT. Furthermore, wiring of the upper part of the capacitative element for information storage may consist of Cu(s) (copper).

[0070]

[Effect of the Invention] It will be as follows if the effect acquired by the typical thing among invention indicated by this application is explained briefly.

[0071] According to this invention, since the wiring layer of a memory array and the wiring layer of a circumference circuit can be reduced, the number of manufacturing processes of DRAM can be reduced and improvement in the yield and reduction of a

manufacturing cost can be aimed at.

[0072] According to this invention, since a gate electrode (word line) can be formed into low resistance, the number of the WORD drivers connected to a predetermined number of memory cells can be reduced, thereby, a chip size can be reduced and the degree of integration of DRAM can be raised.

[0073] the connection formed in the upper part of the source field of these MISFET(s), and a drain field by having arranged the 1st-layer wiring and the 2nd-layer wiring which connect n channel type MISFET and p-channel type MISFET of a circumference circuit in the lower layer rather than the capacitative element for information storage of a memory cell according to this invention -- the aspect ratio of a hole can be made small and the connection reliability of wiring of a circumference circuit can be raised

[0074] According to this invention, since the number of the heat treatment processes of the whole process can be reduced, diffusion of the impurity in the source field of MISFET and a drain field can be suppressed, shallow pn junction can be formed, and detailed-izing of MISFET which constitutes DRAM by this, and highly efficient-ization can be promoted.

[Brief Description of the Drawings]

[Drawing 1] It is the whole semiconductor chip plan in which DRAM which is the gestalt 1 of operation of this invention was formed.

[Drawing 2] It is the expansion plan of the semiconductor chip in which DRAM which is the gestalt 1 of operation of this invention was formed.

[Drawing 3] It is the important section cross section of a semiconductor substrate showing DRAM which is the gestalt 1 of operation of this invention.

[Drawing 4] It is the plan showing a part of circumference circuit of DRAM which is the gestalt 1 of operation of this invention.

[Drawing 5] It is the important section cross section of a semiconductor substrate showing the manufacture method of DRAM which is the gestalt 1 of operation of this invention.

[Drawing 6] It is the important section cross section of a semiconductor substrate showing the manufacture method of DRAM which is the gestalt 1 of operation of this invention.

[Drawing 7] It is the important section cross section of a semiconductor substrate showing the manufacture method of DRAM which is the gestalt 1 of operation of this invention.

[Drawing 8] It is the important section cross section of a semiconductor substrate showing the manufacture method of DRAM which is the gestalt 1 of operation of this

invention.

[Drawing 9] It is the important section cross section of a semiconductor substrate showing the manufacture method of DRAM which is the gestalt 1 of operation of this invention.

[Drawing 10] It is the important section cross section of a semiconductor substrate showing the manufacture method of DRAM which is the gestalt 1 of operation of this invention.

[Drawing 11] It is the important section cross section of a semiconductor substrate showing the manufacture method of DRAM which is the gestalt 1 of operation of this invention.

[Drawing 12] It is the important section cross section of a semiconductor substrate showing the manufacture method of DRAM which is the gestalt 1 of operation of this invention.

[Drawing 13] It is the important section cross section of a semiconductor substrate showing the manufacture method of DRAM which is the gestalt 1 of operation of this invention.

[Drawing 14] It is the important section cross section of a semiconductor substrate showing the manufacture method of DRAM which is the gestalt 1 of operation of this invention.

[Drawing 15] It is the important section cross section of a semiconductor substrate showing the manufacture method of DRAM which is the gestalt 1 of operation of this invention.

[Drawing 16] It is the important section cross section of a semiconductor substrate showing the manufacture method of DRAM which is the gestalt 1 of operation of this invention.

[Drawing 17] It is the important section cross section of a semiconductor substrate showing the manufacture method of DRAM which is the gestalt 1 of operation of this invention.

[Drawing 18] It is the important section cross section of a semiconductor substrate showing the manufacture method of DRAM which is the gestalt 1 of operation of this invention.

[Drawing 19] It is the important section cross section of a semiconductor substrate showing DRAM which is the gestalt 2 of operation of this invention.

[Description of Notations]

1 Semiconductor Substrate

1A Semiconductor chip

2 It is Well P Molds.
3 It is Well N Molds.
4 Field Oxide Film
5 P Type Channel-Stopper Layer
6 N Type Channel-Stopper Layer
7 Gate Oxide Film
8A, 8B, 8C Gate electrode
8D Wiring
9 N-type-Semiconductor Field
10 Silicon Nitride Film
11 Sidewall Spacer
12 N - Type Semiconductor Region
13 N+ Type Semiconductor Region
14 P - Type Semiconductor Region
15 P+ Type Semiconductor Region
16 Ti Silicide Layer
17 Silicon-Oxide Film
18 BPSG Film
19 Silicon-Oxide Film
20 Plug
21 Connection -- Hole
22 Connection -- Hole
23 Connection -- Hole
24 Connection -- Hole
25 Connection -- Hole
26 Connection -- Hole
27 Connection -- Hole
28 Polycrystal Silicon Film
29 Plug
30A-30G Wiring
31 Silicon-Oxide Film
32 Accumulation Electrode (Lower Electrode)
33 Capacity Insulator Layer
34 Plate Electrode (Up Electrode)
35 Plug
36 Connection -- Hole

37 Silicon·Oxide Film

38A·38D Wiring

39A, 39B, 39C Auxiliary wiring

40 Connection ·· Hole

41 Connection ·· Hole

C Capacitative element for information storage

BL1, BL2 Bit line

MARY Memory array

MM Memory mat

Qn N channel type MISFET

Qp P-channel type MISFET

Qt MISFET for memory cell selection

SA Sense amplifier

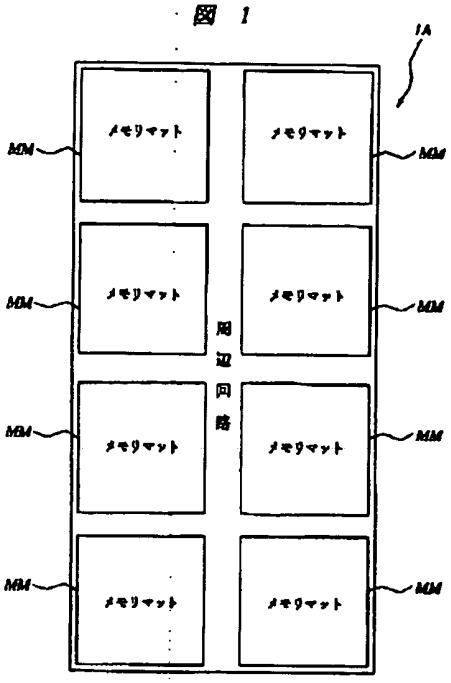
WD WORD driver

WL Word line

YS Y selection line

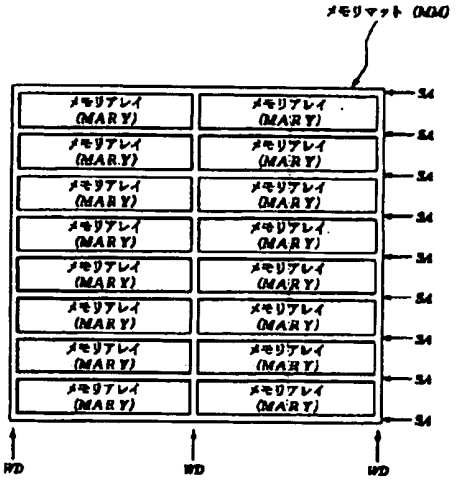
【図１】

図 1



【図２】

図 2



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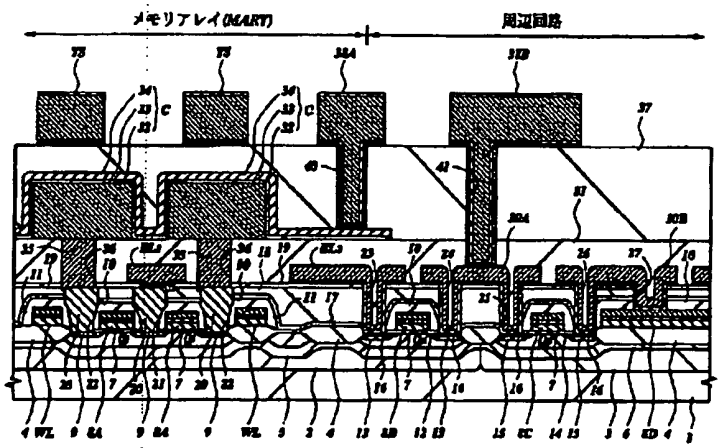

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図 4

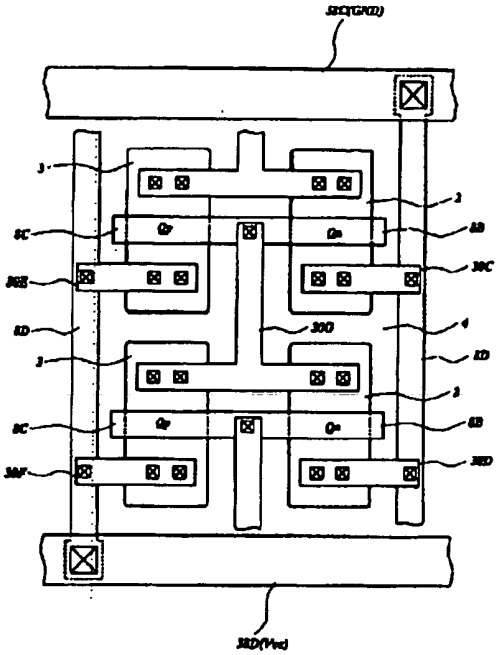

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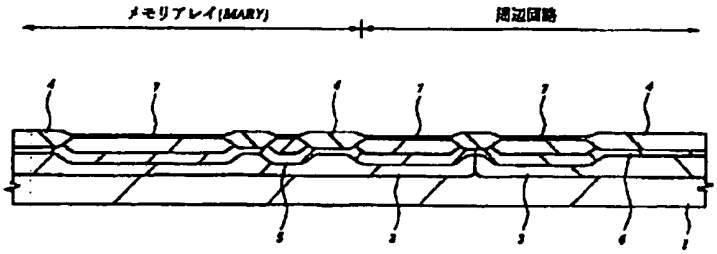
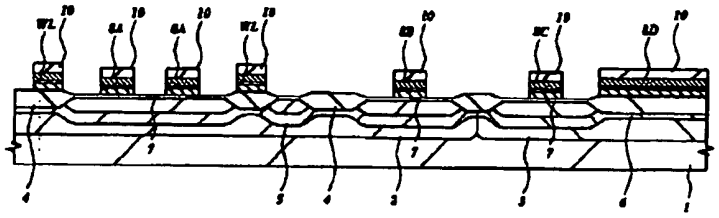
図 5



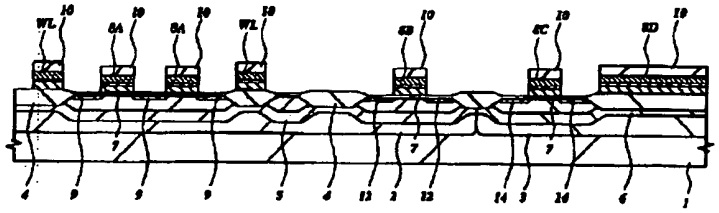
【図6】

図 6



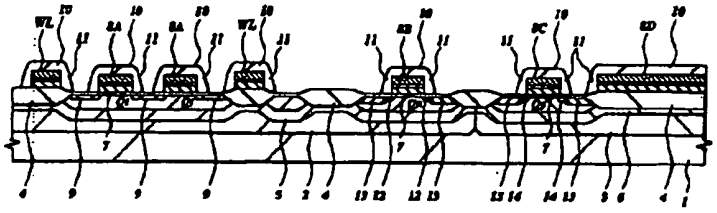
【図7】

図 7



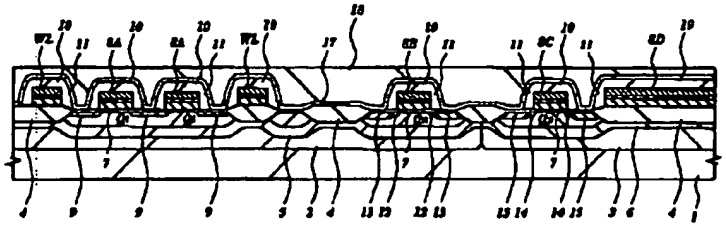
【図8】

図 8



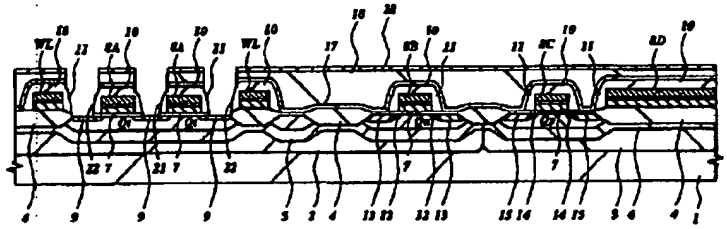
【図9】

図 9



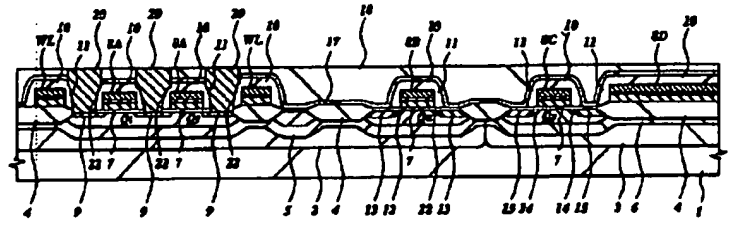
【図10】

図 10



【図11】

図 11



【図12】

図 12

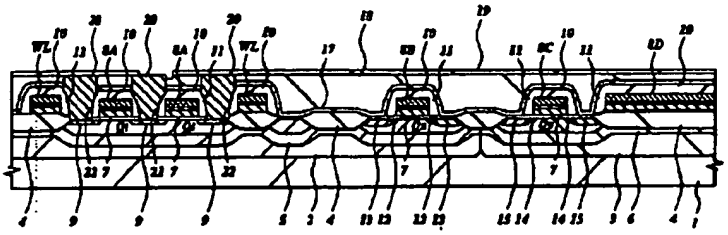


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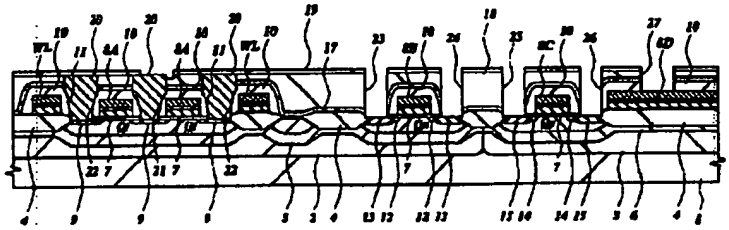
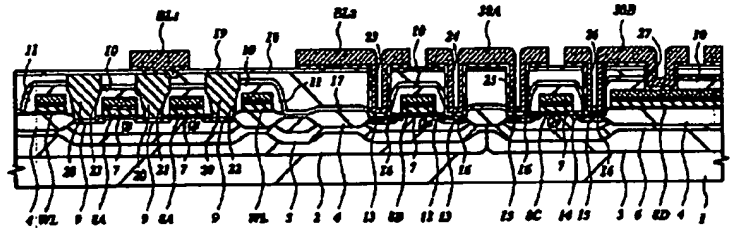
図 13



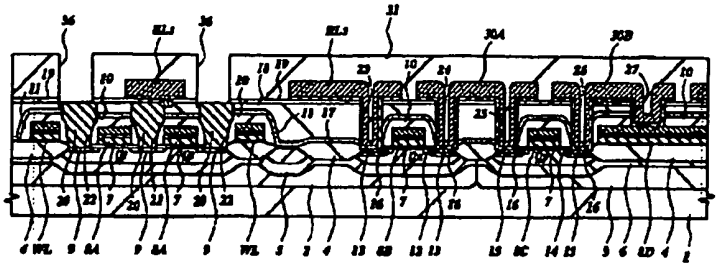
【図14】

図 14



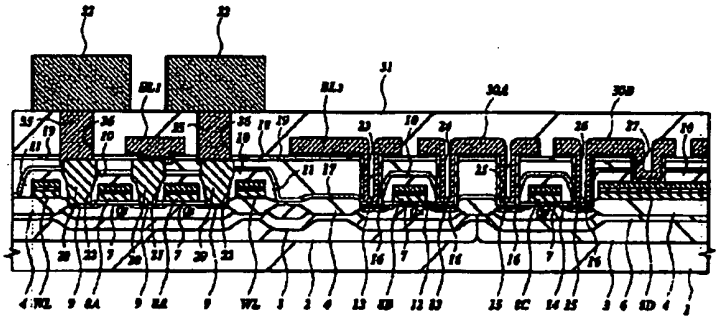
【図15】

図 15



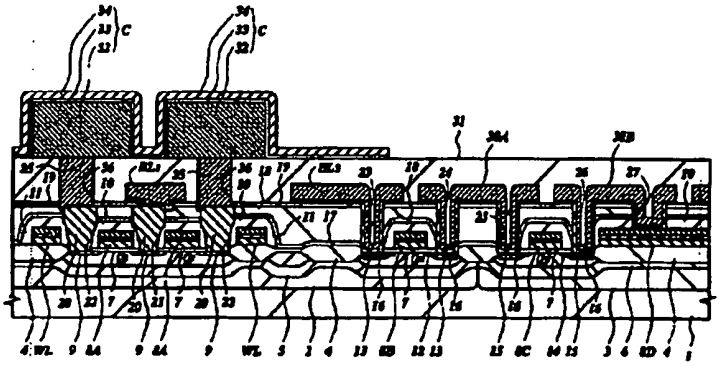
【図16】

図 16



【図17】

図 17



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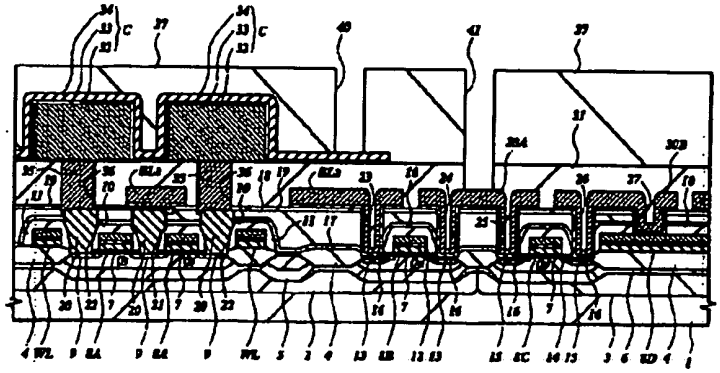
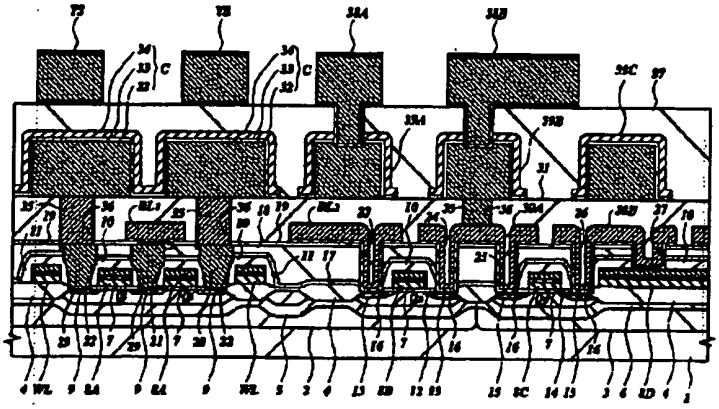


【図19】

図 19



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